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To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
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Poughkeepsie, N.Y. 12603

Subject:

Divisional Patent Application of
Serial No. 10/295,157 11/15/02

Chrong Jung Lin

"A NOVEL MULTI-LEVEL (4STATE/2-BIT) STACKED GATE FLASH MEMORY CELL"

Grp. Art Unit: 2822 Examiner: K. PICARDAT

PRELIMINARY AMENDMENT

Dear Sir:

This is a preliminary amendment for the above referenced Divisional Patent Application. Please amend the above identified application for patent as follows:

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 13, 2004.

Stephen B. Ackerman, Reg. No. 37,761

Signature

Date April 13, 2004

AMENDMENTS TO THE CLAIMS:

If entered, this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1 - 18. (Canceled)

19. (Original) A multi-level, multi-bit stacked gate flash memory cell structure comprising:

floating gate spacers having convex walls facing each other, and vertical outside walls;

a conformal dielectric layer covering said convex walls of said floating gate spacers;

a control gate therebetween said convex walls of said floating gate spacers with intervening said conformal dielectric layer; and

insulative spacers formed on said vertical outside walls of said floating gates.

20. (Original) The stacked gate flash memory cell of claim 19, wherein said floating gate spacers comprise polysilicon having a lateral thickness between about 500 to 2000 Å.

21. (Original) The stacked gate flash memory cell of claim 19, wherein said conformal dielectric layer comprises oxide-nitride-oxide (ONO) having a thickness between about 600 to 1100 °C.

22. (Original) The stacked gate flash memory cell of claim 19, wherein said control gate comprises polysilicon.

23. (Original) The stacked gate flash memory cell of claim 19, wherein said oxide spacers have a lateral thickness between about 1000 to 3000 Å.

24. (New) A multi-level, multi-bit stacked gate flash memory cell structure, comprising:

two floating gates on an insulating layer on a substrate,having opposite sidewalls facing each other;

a conformal dielectric layer covering opposite sidewalls of the two floating gates;

a control gate therebetween the opposite sidewalls of the two floating gates with intervening the conformal dielectric layer; and

two insulative spacers covering outside walls of the two floating gates.

25. (New) The flash memory cell structure of claim 24, further comprising a first, second and third doped regions in the substrate as source/drain regions, wherein the first doped region is disposed between the two opposite sidewalls of the two floating gates, and the second and third doped regions are disposed outside of the outside walls of the two floating gates respectively.

26. (New) The flash memory cell structure of claim 25, wherein the substrate is a p-type semiconductor substrate and the first, second and third doped regions are n-doped regions, and the first n-doped region is served as a source region and the second and third n-doped regions are served as a drain regions.

27. (New) The flash memory cell structure of claim 24, wherein the floating gates and control gate comprise polysilicon.

28. (New) The flash memory cell structure of claim 24, wherein the conformal dielectric layer comprises oxide-nitride-oxide (ONO).

29. (New) A multi-level, multi-bit stacked gate flash memory cell structure, comprising:

two floating gates on an insulating layer on a substrate, having opposite sidewalls facing each other;

a conformal dielectric layer covering opposite sidewalls of the two floating gates;

a control gate therebetween the opposite sidewalls of the two floating gates with intervening the conformal dielectric layer;

two insulative spacers covering outside walls of the two floating gates; and

further comprising a first, second and third doped regions in the substrate as source/drain regions, wherein the first doped region is disposed between the two opposite sidewalls of the two floating gates, and the second and third doped regions are disposed outside of the outside walls of the two floating gates respectively.

30. (New) The flash memory cell structure of claim 29, wherein the substrate is a p-type semiconductor substrate and the first, second and third doped regions are n-doped regions, and the first n-doped region is served as a source region and the second and third n-doped regions are served as a drain regions.

31. (New) The flash memory cell structure of claim 29, wherein the floating gates and control gate comprise polysilicon.

32. (New) The flash memory cell structure of claim 29, wherein the conformal dielectric layer comprises oxide-nitride-oxide (ONO).